

FIG. 1

0002/0" 200603050

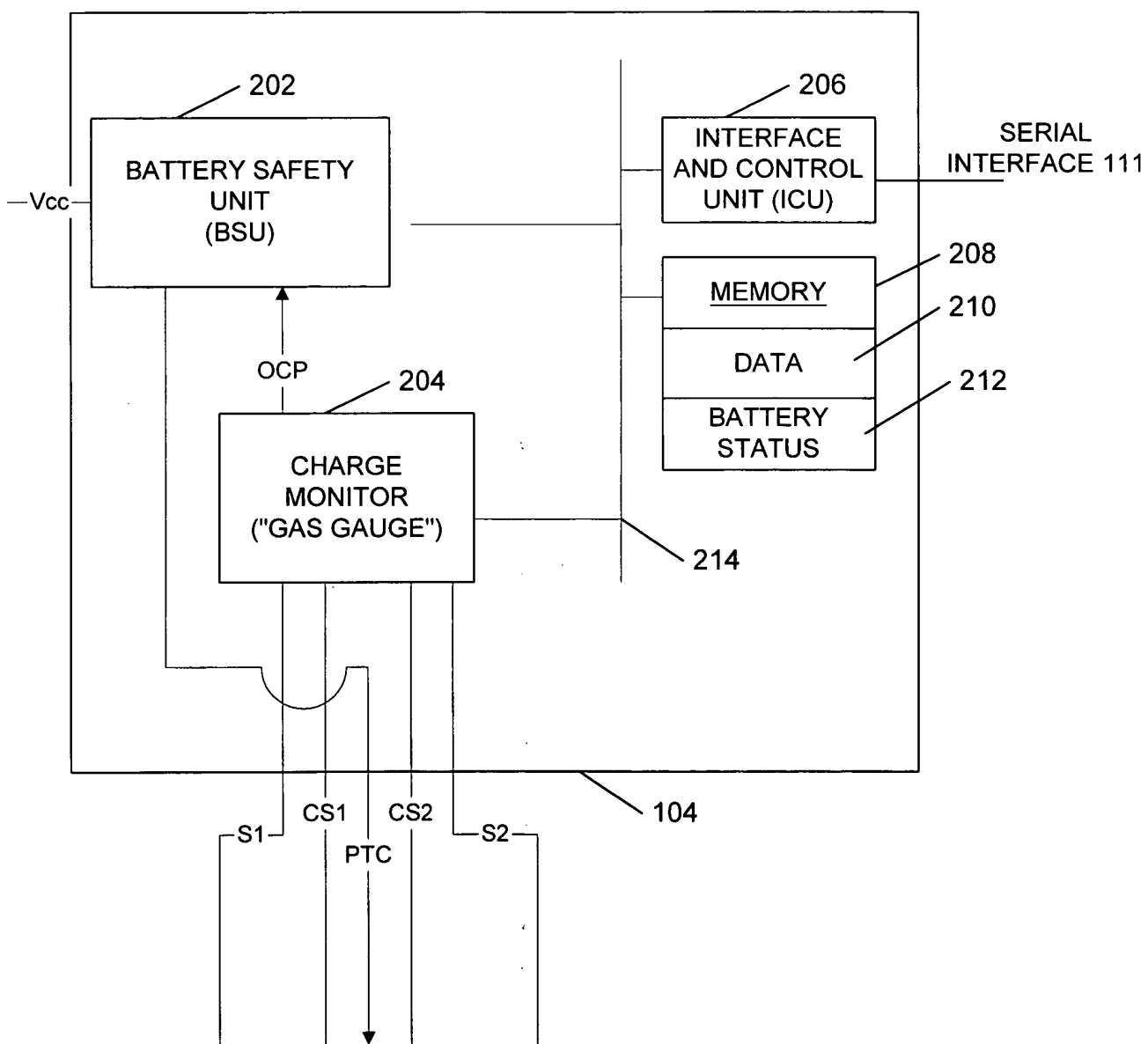


FIG. 2

The diagram illustrates a digital-to-analog converter (DAC) circuit, specifically a current-steering DAC with a feedback loop. The circuit is divided into two main sections: a feedback loop (301) and a DAC core (311).

**Feedback Loop (301):** This section includes a differential pair of transistors (306, 308) with gates connected to a common-mode feedback signal (VB1, 304). The sources of these transistors are connected to a common-mode feedback node (322). The output of the differential pair is connected to a current source (310) and a capacitor (CM). The current source is controlled by a digital input (VB2). The output of the feedback loop is connected to a comparator (CMP1, 302).

**DAC Core (311):** This section includes a differential pair of transistors (312, 316) with gates connected to a common-mode feedback signal (VB3). The sources of these transistors are connected to a common-mode feedback node (318). The output of the differential pair is connected to a current source (310) and a capacitor (CM). The current source is controlled by a digital input (VB2). The output of the DAC core is connected to a comparator (CMP2, 312).

**Control and Timing:** The circuit is controlled by a counter (318) which provides a clock signal (OCP) to the DAC core. The counter also provides a feedback signal (316) to the DAC core. The DAC core is also controlled by a digital input (VB2).

**Input/Output:** The DAC core has two inputs: a digital input (VB2) and an analog input (VB3). The DAC core has two outputs: a digital output (OCP) and an analog output (316).

**Transistor Details:** The transistors are labeled with their gate (G), source (S), and drain (D) connections. For example, transistor 606 has gate (G), source (SF1), and drain (D) connections. Transistor 602 has gate (G), source (F1), and drain (D) connections.

**FIG. 3**

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graph LR; 206[206] --- 404[404 INTERRUPT LOGIC]; 206 --- 406[406 ALARM LOGIC]; 206 --- 408[408 ARITHMETIC UNIT]; 206 --- 402[402 SERIAL INTERFACE LOGIC]; 404 --> 406; 406 --> 408; 408 --> 402; 402 --> 406; 406 --> BUS[TO BUS]; 402 <--> SP[TO SERIAL PORT];
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The diagram illustrates the internal architecture of a microcontroller, designated as 206. It features four primary functional blocks: Interrupt Logic (404), Alarm Logic (406), Arithmetic Unit (408), and Serial Interface Logic (402). These blocks are interconnected within the microcontroller's boundary. Bidirectional data paths are shown between Interrupt Logic and Alarm Logic, Alarm Logic and Arithmetic Unit, and Arithmetic Unit and Serial Interface Logic. Additionally, bidirectional communication is established between Serial Interface Logic and Alarm Logic. The Alarm Logic block has a direct output path labeled 'TO BUS', and the Serial Interface Logic block has a bidirectional connection to a 'TO SERIAL PORT'.

**FIG. 4**

The figure displays four timing diagrams for digital signals, each with a specific label and a set of time intervals:

- START:** The signal transitions from high to low. The duration of the low pulse is  $30\ \mu\text{s}$ . This is followed by a series of eight high pulses, each with a duration of  $30\ \mu\text{s}$ . The signal then transitions back to low for a duration of  $90+\ \mu\text{s}$ .
- ACK:** The signal transitions from high to low. The duration of the low pulse is  $30\ \mu\text{s}$ . This is followed by a series of four high pulses, each with a duration of  $30\ \mu\text{s}$ . The signal then transitions back to low for a duration of  $90+\ \mu\text{s}$ .
- ONE:** The signal transitions from high to low. The duration of the low pulse is  $30\ \mu\text{s}$ . This is followed by a series of three high pulses, each with a duration of  $30\ \mu\text{s}$ . The signal then transitions back to low for a duration of  $90+\ \mu\text{s}$ .
- ZERO:** The signal transitions from high to low. The duration of the low pulse is  $30\ \mu\text{s}$ . This is followed by a series of two high pulses, each with a duration of  $30\ \mu\text{s}$ . The signal then transitions back to low for a duration of  $90+\ \mu\text{s}$ .

FIG. 5

000270-80603960

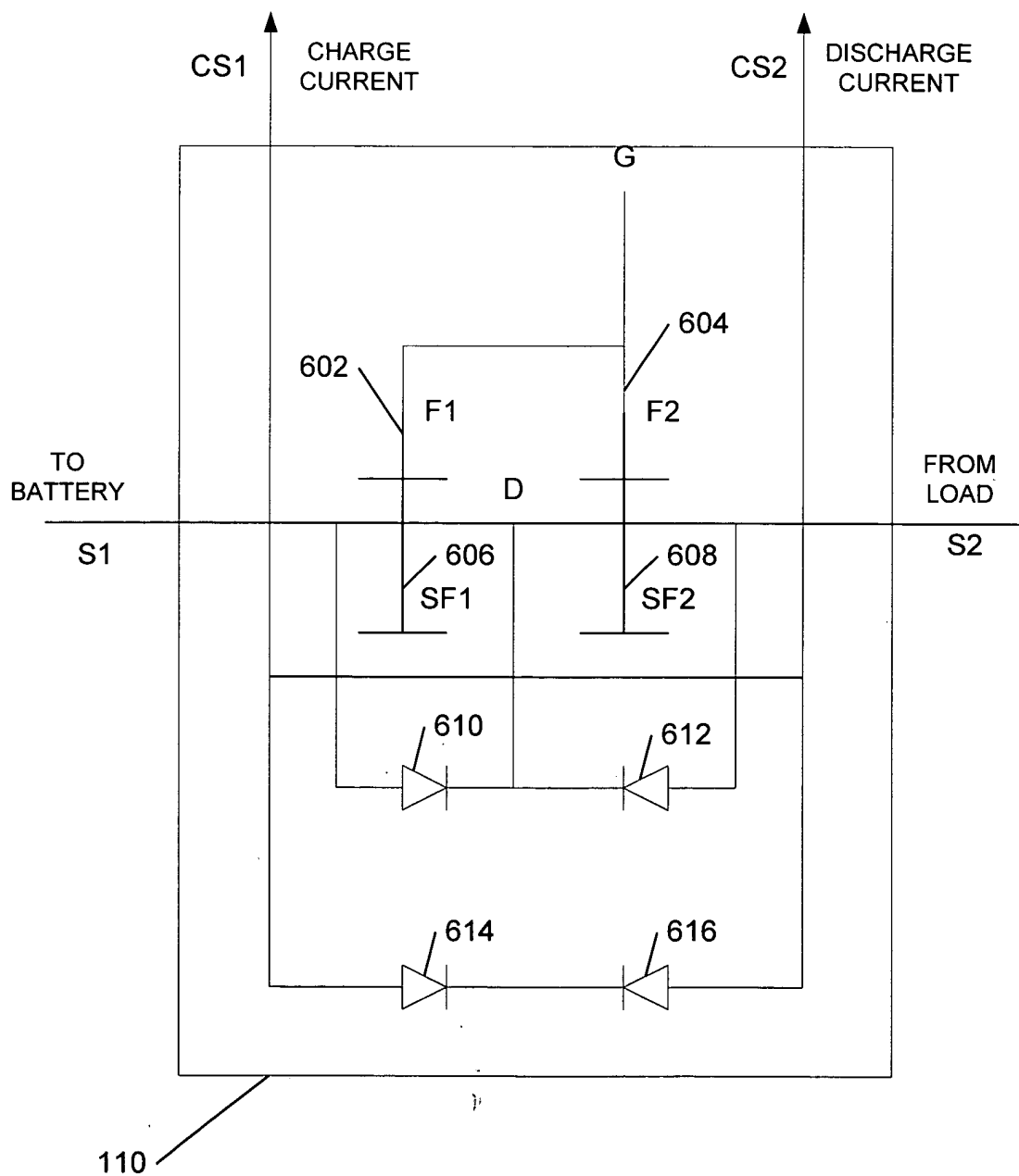


FIG. 6